the Examiner is not persuaded by Applicant's arguments, Applicant respectfully requests that the Examiner enter the Amendment to clarify issues upon appeal.

In the above-identified Final Office Action, the Examiner rejected claims 1-7 under 35 U.S.C. § 103 as being unpatentable over Applicant's admitted prior art ("AAPA") in view of by U.S. Patent No. 5,065,220 ("Paterson"). In response to Applicant's arguments that if Paterson is added to the AAOA, the combination would still fail to teach or suggest that the silicide layer on the first component that resides on the first polysilicon layer does not reside between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks, the Examiner stated that:

> [t]his argument is not persuasive since in the AAPA device, the silicide laye does not reside between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks. The AAPA does not teach a silicide on the tope surface of the polysilicon laye of the at least one component. However, Paterson et al. shows that is is conventional in the art to have a device with a silicide (14) on [the] top surface of the polysilicon layer (12) as mention [sic] above.

Applicant respectfully disagrees with the Examiner's rejection. Claim 1 recites:

> [a] flash memory device comprising:
> a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate;
> at least one component including a polysilicon layer having a top surface;
> a silicide on the top surface of the polysilicon layer of the at least one component;
> an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein, the plurality of contact holes being formed by etching the insulating layer to provide the plurality of contact holes, the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer; and
> a conductor for filling the plurality of contact holes;
> wherein the silicide layer resides on the first polysilicon layer but not between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks.

Thus, although the silicide layer covers the polysilicon layer of the at least one

component, the silicide layer does not cover the layers within the plurality of gate stacks such that the silicide layer is not beween the gates of the gate stack. The flash memory device of claim 1 includes a silicide layer on the first polysilicon layer, but not between the gates of the gate stacks. The silicide layer allows for better electrical contact to the component. Specification, page 13, lines 4-6. Moreover, the silicide layer acts as an etch stop to prevent over-etching of the polysilicon component and destruction of field insulating regions during etching of contact holes. Specification, page 13, lines 1-4.

As the Examiner has acknowledged, the AAPA does not "teach a silicide on the top surface of the polysilicon layer of the at least one component, and the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer." Instead, the AAPA merely discloses the presence of gate stacks and polysilicon components, with contact holes that have been etched in the insulating layer. Specification, page 2, line 22-page 3, line 20 and Figures 2A and 2B. The AAPA is thus completely devoid of mention of a silicide layer on the first polysilicon layer of any component for any purpose.

Paterson describes a semiconductor device including capacitors. Paterson, Abstract, lines 1-3. Paterson states that the capacitor has a "lower plate formed of polycrystalline silicon which, in this embodiment, is clad in a refractory metal silicide 14." Paterson, col. 2, lines 42-45. The capacitor also includes a top plate formed above the lower plate and silicide. Paterson, col. 2, lines 56-58. The silicide layer on the lower plate is provided "for additional stability of the capacitor 2." Paterson, col. 2, lines 49-50. The silicide layer thus resides between the bottom and top plates of the capacitor. Paterson, col. 2, lines 42-58 and Fig. 1. During formation, a first

polysilicon layer is formed, and the silicide formed on that first polysilicon layer for all of the devices, including but not limited to the capacitor. Paterson, col. 3, lines 13-61. The silicide is used to enhance the voltage stability of the capacitor, though the first polysilicon layer of all other structures is also silicided at the same. Paterson, col. 3, lines 54-61 and Figs. 2a-2h (silicide film 14). Furthermore, Applicant can find no indication in Paterson that the silicide layer is removed on the other structures.

The AAPA in view of Paterson fails to teach or suggest a semiconductor device which has a silicide layer on the first polysilicon layer of a device, but not between the layers of gate stacks, which also include a first polysilicon layer. Paterson teaches that the silicide layer is provided on first (lowest) polysilicon all of the devices. For example, in Figures 1 and 2a-2h, all of the devices have the silicide layer 14 on them. Consequently, although the silicide layer of Paterson is provided for the lower plates of the capacitors, it apparently also resides on *all* of the devices of Paterson, including between the plates of the capacitor of Paterson.

Consequently, if the silicide layer of Paterson was used in the AAPA, a first polysilicon layer would be deposited and silicided. This silicide layer would remain on the first polysilicon layer of all devices, including the gate stacks and any capacitors. Other layers would be provided on this silicided polysilicon layer to form devices. Thus, this silicided polysilicon layer would typically be present within the gate stacks, for example as the floating gate, and within other devices such as capacitors. Consequently, a portion of the silicide layer would reside between the floating gate and the control gate in each gate stack. This is contrary to the silicide layer recited in claim 1 and described in the specification. As a result, even if the teachings of Paterson are added to those of the AAPA, the combination would still fail to teach or suggest that

the silicide layer on the first component that resides on the first polysilicon layer does not reside between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks. The AAPA in view of Paterson, therefore, cannot teach or suggest the flash memory device recited in claim 1. Accordingly, Applicant respectfully submits that claim 1 is allowable over the cited references.

Furthermore, Applicant respectfully disagrees with the Examiner's response to Applicant's arguments and respectfully submits that the Examiner's response to Applicant's arguments involves impermissible hindsight. It is well established that one "cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also In re Fritch, 23 USPQ2d 1780,1783 (Fed. Cir. 1992). In the response, the Examiner appears to rely on the fact that the AAPA does not describe a silicide layer between the layers of the gate stack. However, the AAPA does not describe any silicide layer on the first polysilicon layer. The reference used by the Examiner to teach a silicide layer, Paterson, indicates that the silicide layer would be present on the first polysilicon layer of all devices. Applicant respectfully submits that the use of Paterson to teach the (missing) silicide layer of the AAPA and the AAPA to teach that the silicide layer is not provided between the layers of the gate stack involves impermissible hindsight. Consequently, Applicant respectfully submits that claim 1 is allowable over the cited references.

Claims 2-7 depend on independent claim 1. Consequently, the arguments herein apply with full force to claims 2-7. Thus, Applicant respectfully submits that claims 2-7 are allowable over the cited references.

In view of the foregoing, it is submitted that the claims in the application are patentable over the cited reference and are in condition for allowance. Reconsideration of the rejections and objections is requested.

Applicants' attorney believes this application in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

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Date

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